REMARKS

This paper is responsive to Non-Final Office action dated May 1, 2006. Claims 1-22 and 24-42 were examined. Claims 26-40 are allowed. Claims 1-3, 8, 13, 15, 24, 25, 41 and 42 stand rejected. Claims 4-7, 9-12, 14 and 16-22 are objected to.

Claim Rejections Under 35 U.S.C. § 102(b)

Claims 41-42 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,038,187 issued to El Hajji (hereinafter "El Hajji"). Regarding claim 41, Applicants respectfully maintain that El Hajji, alone or in combination with other references of record, fails to teach or suggest

> means for detecting in situ a sensing offset in a sensing circuit that includes a cross-coupled pair of transistors,

as required by claim 41. El Hajji teaches a circuit for measuring a voltage across the terminals of a storage capacitor in a memory circuit to detect voltage decay due to leakage currents and refreshing the memory circuit in response to detection of the voltage being lower than a predetermined voltage. Col. 2, lines 2-10; col. 8, lines 33-43. Nowhere does El Hajji teach or suggest means for detecting in situ a sensing offset in a sensing circuit that includes a cross-coupled pair of transistors, as required by claim 41. For at least this reason, Applicants respectfully maintain that claim 41 distinguishes over El Hajji and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 41 and all claims dependent thereon, be withdrawn.

Claim Rejections Under 35 U.S.C. § 102 (e)

Claims 1-3, 8, 13, 15, 24-25 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pub. No. 2004/0008534 issued to Kurth et al. (hereinafter "Kurth").

Regarding claim 1, Applicants respectfully maintain that Kurth, alone or in combination with other references of record, fails to teach or suggest

> a test block for a memory circuit, wherein the test block is configured to characterize in situ a sensing offset of a sensing circuit including a cross-coupled pair of transistors,

as required by claim 1. Kurth teaches a ROM-embedded DRAM that includes ROM cells that can be programmed to a single state. Abstract. A series of gate control transistors 211 of Kurth set a bias to couple NLAT1 and NLAT2 to transistors Q3 and Q4 of n-sense amplifier 212. [0040]; FIG. 4.

> In one embodiment, $NLAT_1$ is at a potential of Vcc/2 (or DVC2) and $NLAT_2$ is at a potential of Vcc/2+ (or DVC2+), slightly greater than DVC2. In one embodiment, DVC2+ is approximately 50 millivolts (mV) higher than the potential of DVC2. These potentials are placed on the respective n-sense amplifier bus lines, RNL*A or RNL*B depending on which bias, 208A or 208B, is selected. Thus, NLAT is at a potential of DVC2 and $NLAT_2$ is at a potential of DVC2+ when bias 208A is chosen. N-sense amplifier bus lines, RNL* is biased to DVC2 and RNL*B is biased to DVC2+. ACT 270 meanwhile is biased to Vss or signal ground. The digitlines are both initially equilibrated at Vcc/2. Thus, the n-sense amplifier transistors and p-sense amplifier transistors are off. When the memory cell is accessed, a signal develops across the complementary digitline pair. While one digitline contains charge from the cell accessed, the other digitline does not and serves as a reference for the sensing operation.

[0040] Thus, the teachings of Kurth introduce a sensing offset. [0040-41] The offset of the memory sense amplifier of Kurth is introduced by gate control transistors 211. [0040-41] Nowhere does Kurth teach or suggest characterizing the offset of the cross-coupled pair of transistors in the memory sense amplifier of Kurth. For at least these reasons, Applicants respectfully maintain that claim 1 distinguishes over Kurth and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 1 and all claims dependent thereon, be withdrawn.

Regarding claim 5, Applicants respectfully maintain that Kurth, alone or in combination with other references of record, fails to teach or suggest that

> a sensing offset results, at least in part, from an accumulated data-dependent mismatch in characteristics of the cross-coupled transistors,

as required by claim 5. Kurth teaches a series of gate control transistors 211 that introduce a sensing offset. [0040-41] Nowhere does Kurth, alone or in combination with other references of record teach or suggest that the offset of the memory sense amplifier results from an accumulated data-dependent mismatch in characteristics of the cross-coupled transistors, as claimed and described in the specification at least in paragraph 1019. For at least this reason, Applicants respectfully maintain that claim 5 distinguishes over Hush and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 5 and all claims dependent thereon, be withdrawn.

Regarding claim 8, Applicants respectfully maintain that Hush, alone or in combination with other references of record, fails to teach or suggest

> at least a first and a second discharge path coupled to at least one of the respective first and second plurality of ports, the effective strengths of the first and second discharge paths determined by respective ones of the first and second plurality of control signals, the first and second discharge paths configurable for characterization of a sensing offset associated with a sensing circuit,

as required by claim 8. Kurth teaches a ROM-embedded DRAM that includes ROM cells that can be programmed to a single state. Abstract. A series of gate control transistors 211 of Kurth set a bias to couple NLAT1 and NLAT2 to transistors Q3 and Q4 of n-sense amplifier 212. [0040]; FIG. 4.

> In one embodiment, $NLAT_1$ is at a potential of Vcc/2 (or DVC2) and $NLAT_2$ is at a potential of Vcc/2+ (or DVC2+), slightly greater than DVC2. In one embodiment, DVC2+ is approximately 50 millivolts (mV) higher than the potential of DVC2. These potentials are placed on the respective n-sense amplifier bus lines, RNL*A or RNL*B depending on which bias, 208A or 208B, is selected. Thus, NLAT is at a potential of DVC2 and $NLAT_2$ is at a potential of DVC2+ when bias 208A is chosen. N-sense amplifier bus lines, RNL* is biased to DVC2 and RNL*B is biased to DVC2+. ACT 270 meanwhile is biased to Vss or signal ground. The digitlines are both initially equilibrated at Vcc/2. Thus, the n-sense amplifier transistors and p-sense amplifier transistors are off. When the

> memory cell is accessed, a signal develops across the complementary digitline pair. While one digitline contains charge from the cell accessed, the other digitline does not and serves as a reference for the sensing operation.

[0040]. Thus, the teachings of Kurth introduce a sensing offset. [0040-41] The offset of the memory sense amplifier of Kurth is introduced by gate control transistors 211. [0040-41] Nowhere does Kurth teach or suggest characterizing the offset of the cross-coupled pair of transistors in the memory sense amplifier of Kurth. For at least this reason, Applicants respectfully maintain that claim 8 distinguishes over Kurth and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 8 and all claims dependent thereon, be withdrawn.

Allowable Subject Matter

Applicants appreciate the indication of allowable subject matter in claims 4-7, 9-12, 14, 16-22. Applicants believe that claims 4-7, 9-12, 14, 16-22 depend from allowable base claims and are allowable for at least this reason.

Applicants appreciate the allowance of claims 26-40.

In summary, claims 1-22 and 24-42 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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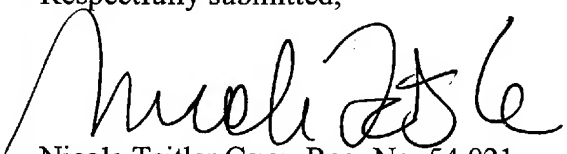

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